

THE MYSTERIOUS WORKINGS OF ANALOG/.DISCHARGE

Rev C

The Agilent 3070 series of board testers have quite a few features built into both the hardware and software to make developing board tests easier, while protecting the operator, the board under test, and the 3070 itself, from harm. One of these features is the discharge routine written by IPG during program development to insure that all capacitors on the board under test do not retain potentially harmful residual voltages.

The discharge routine is found in the analog directory as a file called .discharge (notice the preceding decimal point, it IS important). This file contains information that allows the tester to discharge capacitors on the board under test that could potentially cause difficulties. Note that the capacitors may already be charged when the board is placed on the fixture; or they may charge as a result of applying sources during in-circuit tests, or applying the DUT power supplies during powered testing.

This article was created to enable you to get a better understanding of how the automatically generated discharge routine works. It will also give you information to help you deal with unusual circumstances that the IPG program generator doesn't handle in an optimum fashion.

WHAT CAPACITORS ARE PUT IN THE FILE?

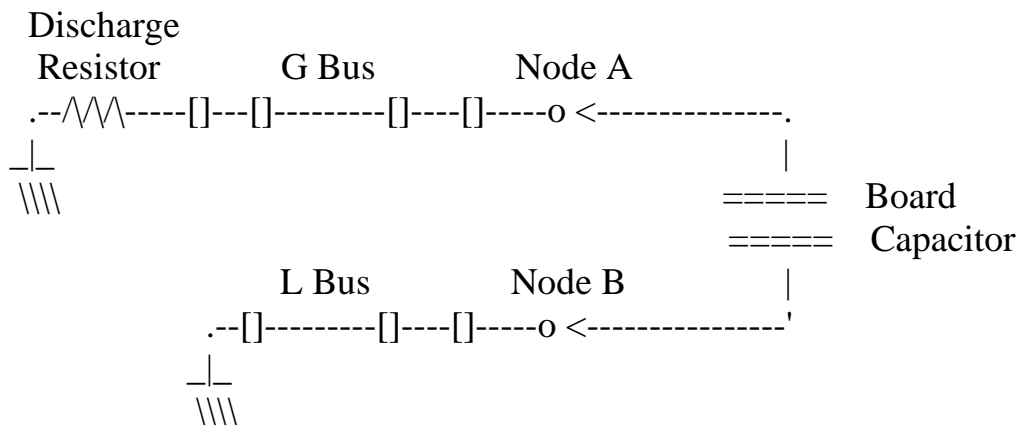
When Test Consultant is run, the system (IPG actually) adds together the absolute values of all the power supply voltages defined in board forms. For example if -12, +5, and -5 volt supplies are defined, the system will assume the maximum capacitor charge voltage to be 22 volts. It then assumes that maximum voltage can appear across ANY of the capacitors defined in board forms.

Next it calculates the maximum power for each capacitor using the formula $P=.5*C*V*V$. If the resultant power is OVER 200 u joules, it puts that capacitor into the discharge routine. Note that if the capacitor has inaccessible nodes it is still put into the discharge routine, but it's commented.

HOW DOES THE ROUTINE WORK?

The discharge routine uses the L Bus and G Bus as modeled roughly below to perform the capacitor discharge. All the circuitry shown is located internal to the 3070, with the exception of Node A and Node B which are points on the board under test, and the "board capacitor". Note that the discharge resistor (whose automatically selected value depends on the voltage measured on the board) is ALWAYS connected via the G Bus, and the path to ground is ALWAYS

completed by the L Bus. The symbol [] indicates a relay internal to the 3070.



If the board capacitor is connected to a fixed node on either end, the L Bus will be automatically be connected to the capacitor node closest to ground (from software revision B2.50 on, see Appendix A).

WHEN DOES IT RUN?

1. Commands which run a full discharge (a full discharge will make up to 4 attempts to reduce the capacitor voltage below 0.05 volts.):
 - a) The 'unpowered' command.
 - b) Commands to engage vacuum ('faon', 'fbon', etc.); IF the current test mode is unpowered.
 - c) Fixture verify commands (for example 'verify all nodes') if the mode is powered.
 - d) Executing the command test "analog/.discharge"

2. The 'dps' command will run a partial discharge (make only 1 attempt to reduce the voltage below 0.05 volts) after the power supplies have been discharged to zero volts. The following commands will automatically perform a 'dps' at the time the command is performed (subject to the given requirements):
 - a) 'run' command
 - b) Commands to disengage vacuum ('faoff', 'fboff', etc.)
 - c) 'scratch board' (if cps has already been executed).
 - d) 'load board' (only if change occurred since last load board, or load board caused an error).

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- e) 'fixture lock' and 'fixture unlock' (if cps has already been executed).
- f) 'cps' (if cps has already been executed).
- g) 'dps'
- h) 'powered' and 'unpowered' (if cps has already been executed).
- i) 'autoadjust', and 'confirm'
- j) Any command or test during which ASRU overvoltage error or testhead exception occurs.
- k) 'testhead is *' (if testhead is 1, and vacuum is on or cps has been issued).
- l) 'testhead is 1', 'testhead power on', and 'testhead power off' (if testhead is 1 already).

WHEN DOES IT NOT RUN?

The following items will all cause a testhead exception to be raised. The subtest name and error message will be printed on the report device. If more than one subtest has an exception condition, only one of the exception classes will be raised.

1. If the voltage measured between the two nodes was too high to discharge.
Greater than 100.0 volts on systems with Revision C ASRU cards.
Greater than 50.0 volts on systems with ASRU cards prior to Revision C.
2. Discharge was aborted due to a voltage decrease of less than 20 millivolts per second.
3. Discharge timeout. Each discharge subtest must complete in 29.5 seconds.
4. If the system is unable to measure the discharge voltage.
5. If an over-voltage error condition occurs in the testhead.
6. On a full discharge only, if discharge test has been executed four times, and voltage is still greater than 0.05 volts.

ARE POWERED AND UNPOWERED TESTS DIFFERENT?

The actual routine varies slightly depending on whether the board was in the powered or unpowered mode.

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1. If the system is in the "unpowered" (non functional) mode, and a discharge is caused, the sequence is:
 - a) Discharge the capacitors listed in the discharge file (by running all discharge tests).
 - b) If unsuccessful, raise an exception as explained above (under When Does It Not Run).
 - c) If successful, connect all nodes together simultaneously and check for a short to ground.

To do this the system connects all mint pins on all pin cards in a module to the G Bus at the same time. Then it checks for a short between the G Bus and system ground. It measures for up to one second in that module until it gets three passing measurements. It does this one module at a time.

2. If the system was in the "unpowered; functional" mode (added in B2.75) the sequence is exactly as given in 1 above EXCEPT that the presence of any shorts are ignored.

Note that you can execute the command IPG on ".discharge" to add this feature on routines created before B2.75. It is NOT added automatically when you update to B2.75.

3. If the system was in the "powered" mode, and a discharge is caused, the sequence is:
 - a) First store the states of all GP relays.
 - b) Next open up all switched ground relays and GP relays.
 - c) Then discharge the capacitors listed in the discharge file.
 - d) Finally return GP relays back to their previous state, and close all switched ground relays.
 - e) Note that the mint pins are NOT connected together as they were in the unpowered mode.

WHAT ABOUT PANELIZED BOARDS?

The discharge tests for each board on the panel (1:.discharge, 2:.discharge, etc.) are run together at the same time that a single discharge test would be run. The results are then analyzed for all of the discharge tests as if they came from a single test. If any one of the discharge tests has subtests which "don't run" as outlined above, all discharge tests are treated as one test (all redone, or all stop).

WHAT ABOUT BOARD HANDLERS?

IMPORTANT: There are NO board handler commands that automatically do a discharge. Handler Testmains created by Agilent use the unpowered command to create a discharge.

For a system with a board handler, the commands 'handler press to all probes', 'handler press to long probes', and 'handler press to transfer' are somewhat analogous to 'faon' and 'faoff'. The analogy is not exact because of the dual-stage probes. If you create your own board

handler testplan, a discharge should be implemented between points in the following chart.

<u>Current press location</u>	<u>Next press location</u>
Transfer	All probes
Transfer	Long probes
All probes	Long probes
All probes	Transfer
Long probes	Transfer
Long probes	All probes

SO WHAT COULD GO WRONG?

In the normal course of testing boards the methods outlined above work fine. There are cases however where a little extra work on the programmers' part is necessary.

1. If the board under test contains a voltage converter which produces voltages higher than those supplied by the system power supply settings, for example a DC to DC converter, you will need to make a few modifications. While initially it might seem that one could simply purposely misstate the voltages used in board forms, this method wouldn't create 'fixed nodes' in the right location. While these could be added manually, an easier method is to tell "board" that a power supply with the appropriate voltage is connected to the output of the DC to DC converter. This will allow IPG to create a proper discharge file, as well as to assign fixed nodes correctly. If this is done, make sure that these "phantom" power supply wires are NOT added to the fixture, and thereby avoid potential damage to the board under test.
2. Prior to software revision B.2.50 in the Series II (and on all Series I) the L Bus was not automatically connected to the capacitor node closest to ground. If a capacitor node on the board under test is somehow connected to an external ground, and the discharge routine used the G Bus to ground on that capacitor node, damage could result (see Appendix A). Even on current systems, if ground is separated by a low value of impedance from a capacitor node, it is possible for damage to occur. When in doubt, consider doing the following;

If an analog/.discharge subsection contains a fixed node on one side of a capacitor, you should ALWAYS CONNECT the L BUS to whichever node is closer TO GROUND on that capacitor.

When any capacitor already in the analog/.discharge routine is isolated from a fixed node by a low impedance, consider manually modifying its analog/.discharge subsection, if necessary, so the L Bus is connected to the node closest to ground.

3. The discharge routine could actually be in error if an ECO has occurred and someone has mistakenly used the permanent option on the discharge file in testorder. It is STRONGLY

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RECOMMENDED that the permanent option NEVER BE USED with the discharge file.

4. It is important to note that the automatically generated routine only discharges capacitors. If an inductor (or any other device) on the board under test has significant internal capacitance, you either need to enter that capacitance in the board forms, or perhaps create your own entry in the discharge file.

5. Large capacitors, especially electrolytics, have what is sometimes referred to as dielectric memory, or dielectric absorption. If they are charged up, discharged, and then left alone, a voltage will build up (bounce back) on the capacitor. Note that the voltage built up is not only a function of the voltage previously applied, but also the length of time it was applied. In cases like these it may be necessary to discharge the capacitor several times, perhaps at both the beginning and end of the discharge file (note that the discharge file can be edited as easily as any text file. Be sure you understand what you are doing before starting however.). In extreme cases it may be necessary to add a bleeder resistor or GP relay across the capacitor inside the fixture. The unpowered command runs the discharge test up to four times, checking the voltages on the board before each test, specifically so it can do a better job in removing "bounce-back" charges on the board. If this is not sufficient, you could create a loop of your own within the testplan.

6. You have angered the Gods.
 - a) An exception was raised when Discharge tried to run, and improper actions were taken. Anytime an error occurs during the discharge routine it should be carefully analyzed to determine the reason. Just continuing to test boards normally results in either damaged boards, or a damaged tester.

 - b) A command that does only a partial discharge occurred, and a partial discharge was not enough. Instances like these are hard to find, but 6a above usually illuminates them. Note that it is possible to invoke commands such as unpowered twice if desired, or to simply execute the command test "analog/.discharge" at any desired point.

I'VE DONE EVERYTHING ABOVE, BUT I STILL BLOW BOARDS/RELAYS

There are actually several other things besides an improper DISCHARGE routine that can cause damage to the boards under test or to the 3070. Many times these problems are attributed incorrectly to the discharge routine, and thus solving them becomes more difficult.

1. Inrush and Outrush Current From System Power Supplies.
Different model power supplies have different operating characteristics. In some cases these

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operational differences can cause problems. For example does your supply limit the current when it is first set? Most likely it does not, because most customers wish their board powered up in minimum time, and capacitive inrush can be large. Could this cause a testing problem? Perhaps.

When you set the power supply to zero, what is the current limit? Do you care? Perhaps.

Are there things you can do? Yes. Start by reading Application Note "Up-and-Down Programming DUT Power Supplies" located in the secure area of the Agilent board test internet site <http://www.ate.agilent.com/emt/members>. Finally remember that you could always put a resistor in series with the power supplies to limit the current if desired.

2. Fixture electronics.

If the fixture contains any electronics, especially capacitors that the system doesn't know about, you could have problems. IPG will only create discharge tests for capacitors entered in board forms. This can be a real hard one to get around, but it is possible. Consider such things as entering the fixture electronics into board forms, fixture electronics discharge paths, special discharge subroutines, etc.

3. External Power Supplies.

In some cases it is advantageous to use power supplies that are not entered in "board". This must be done carefully for two reasons. First because the resetting of the supply to zero will not be automatic. In cases like this EVERY possible method of exiting a test must be trapped (break, abort, errors, etc), and a routine written to disconnect the external supply. This is NOT an easy task, and any overlooked exits could cause problems. As an alternative a fixture relay, energized by one of the internal DUT supplies, could have its contacts used to disconnect an external supply automatically whenever that particular internal supply is turned off or disconnected. The second problem is that the system may not create the proper fixed nodes or discharge file if voltages are present on the board under test that the system software doesn't know about.

4. Devices connected via Agilent Performance Port or flying leads.

This is similar to 2 above, and must be similarly handled. Performance Port connections must be considered especially carefully if they are carrying high voltage (up to 622 volts peak is allowed) and/or high current (up to 20 amps is allowed) using the high power block.

5. Powered tests added before the Setup_Power_Supplies subroutine.

It is not unknown for the following sequence of tests to be used;

```
unpowered  
call Shorts  
call Analog_Tests
```

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```
powered
test Analog_No_Suppys_Functional_Test    !*** added powered test
                                           !*** add "test Dummy" here

call Setup_Power_Supplies
call Digital_Tests
call Analog_Functional_Tests
```

All of the categories except the "Analog_No_Suppys_Functional_Test" are standard. The added category is a powered test where no DUT Supplies are turned on. An example would be a relay test, where the ASRU source is used to energize the relay.

In the case shown above there is a real danger of damaging the 3070. Since the 3070 only removes test connections with the occurrence of the NEXT test statement, any connections made in the test Analog_No_Suppys_Functional_Test will be left connected when the DUT Power Supplies are turned on. In order to insure that no problems are created in this manner, Agilent recommends the addition of a "Dummy" analog functional test (this type test has the fastest execution time) just before the Setup_Power_Supplies subroutine is called. The Dummy test only needs to contain the commands "test powered analog" and "end test" in order to compile and execute.

6. Using BRC's.

There are cases where entering BRC's instead of nodes in a test is useful. The problem is that there is no automatic checking for conflicts. You can create havoc really really easily.

7. Swapping S and I in Debug.

The S and A buses are a pair; as are the I and B buses. If a test exists which uses these four buses, and you manually reverse the S and I buses during debug without also reversing the A and B buses, you may easily damage 3070 cards.

8. Discharging Power Supply Nodes Using DUT Supplies.

In order to discharge power supply nodes with 'trapped charges', you can use the system power supplies themselves. Unfortunately there is no simple software command to allow testing for trapped charges. If using this method to discharge power nodes connected to large capacitors, it's a good idea to use the "rps" command to insure the supply has indeed discharged the node before proceeding (and remember to watch out for dielectric absorption).

9. Slow Pull Down of the Board with FAON.

In the current version of testmain (or a current testplan, which is created from testmain by IPG), the first "faon" is done on a line that reads;

```
if Tests_On_This_Board = 1 then faon 0
```

The "0" means "don't wait the normal 1.5 seconds after an faon, just carry right on to the next statement". The next statement happens to be "unpowered" which calls the discharge routine

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among other things. If the vacuum on the system is a bit slow and the discharge routine (called by the unpowered command) is run before the board is in contact with the fixture, then an incomplete discharge could occur.

In fact the worst case scenario would be to hit Start (to rerun the testplan) while debugging a powered test on a board containing large capacitors. If a slow vacuum pull down allowed the unpowered "discharge" to be bypassed, 3070 hybrid card damage will almost certainly occur.

10. Sometimes a testplan will end with a digital or mixed test that makes use of the systems built in pull-up or pull-down "loads". If the testplan then attempts to do a discharge before the board is replaced, the discharge routine may produce an error. Since the 3070 only removes test connections with the occurrence of the NEXT test statement, any connections made in the last test will still be connected when the system tries to run the discharge routine. In some conflict situations, the routine will error out. In cases where this occurs, Agilent recommends the addition of a "Dummy" analog functional test (this type test has the fastest execution time) as the very last powered test in the testplan. The Dummy test only needs to contain the commands "test powered analog" and "end test" in order to compile and execute.

CAN I CREATE MY OWN DISCHARGE SUBROUTINE?

As stated previously, the discharge file is a simple text file, and is easily edited. **EXTREME CARE** should be taken if editing the discharge file, since errors could cause significant damage to boards under test, damage to 3070 boards, and perhaps even imperil the operator.

Each discharge subroutine looks similar to the following;

```
! Capacitor "c13 100n"  
!  
! Maximum capacitance = 120n; damage voltage = 57.74v  
clear connect l to "RGND"  
connect g to "20HZ"  
discharge "CD1", entry 57.7, exit 0.05
```

The first three lines are comments, giving the reference designator and the parts value as entered in board forms, as well as the maximum capacitance determined by the tolerance entered in board (or the sum of all parallel capacitance's it calculates), along with the voltage necessary to create 200 u joules of energy for that size capacitor.

The next two lines indicate the nodes to be "clear connected" to in order to discharge the capacitor.

The final line lists first the subroutine designator "CD1". It then lists the entry voltage, which should be equal to the "damage" voltage. Note that if it is **IMPOSSIBLE** for the entry voltage **EVER** to occur, even under fault conditions, on that particular part, then that test could actually

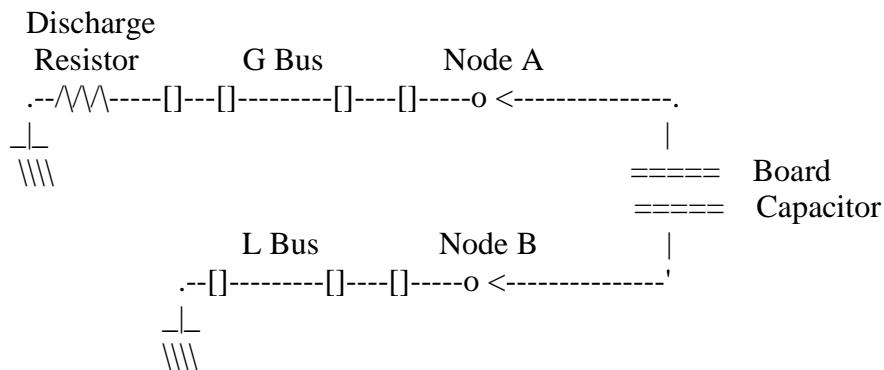
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be eliminated. What the test does is measure the voltage across the two nodes in question when that subroutine is called. If the voltage is BELOW the ENTRY voltage, no further action is taken, and the next discharge subroutine is started. If the measured voltage EXCEEDS the ENTRY voltage, then the system attempts to discharge the part until the EXIT voltage, or an exception, is reached.

With the above information, it is easy to create your own tests. Note that it is possible to add waits, loops, GP Relay connects and disconnects, etc, within the discharge subroutines.

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All the circuitry shown is located internal to the 3070, with the exception of Node A and Node B which are points on the board under test, and the "board capacitor". Note that the discharge resistor (whose value depends on the voltage measured on the board) is ALWAYS connected via the G Bus, and the L Bus ALWAYS completes the path to ground. The symbol [] indicates a relay internal to the 3070.



Note that connecting the L Bus (Node B above) to ground with a clip lead, GP relay, external instrument, etc, will NOT cause a problem. If however a clip lead is connected from the G Bus (Node A above) to ground it will actually short out the discharge resistor located on the ASRU card, presenting a dead short across the two nodes whenever discharge is invoked. If a charged high power capacitor is located between Node A and Node B, and a clip lead is present from Node A to ground, 3070 damage WILL OCCUR.

A modification to automatically incorporate the RULE outlined above into the automatic analog/.discharge routine generation was incorporated in software release B.2.50 in the Series II.

It is NEVER recommended that the permanent option be used on .discharge routines because the danger of system damage due to an ECO is very high.

It is the customers' responsibility to decide if manual modification of the discharge routine is necessary for their particular board to comply with the SUGGESTION outlined above. Note that this type of modification will rarely be needed, it only applies when a charged high power capacitor is isolated from a fixed node by a low impedance.

Example section of an analog/.discharge file;

INCORRECT METHOD

```
-----  
clear connect l to "+24v"  
connect g to "gnd"  
discharge "CD8", entry 577m, exit 0.05
```

CORRECT METHOD

```
-----  
clear connect g to "+24v"  
connect l to "gnd"  
discharge "CD8", entry 577m, exit 0.05
```